Amendments to the Specification:

Please replace the paragraph beginning at page 3, line 6 with the following amended paragraph:

C1 Figure 3 ~~and 4~~ is a schematic block diagram of accelerated graphics port (AGP) functionality of a graphics memory controller hub.

Please replace the paragraph beginning at page 5, line 10 with the following amended paragraph:

Referring to Figures 3 ~~and 4~~, AGP transactions are run in a split transaction fashion in which a request for data transfer to or from system memory 4 is disconnected in time from the data transfer itself. An AGP compliant graphics device (bus master) 7a initiates a transaction with an access request. The AGP interface 21 responds to the request by directing the corresponding data transfer at a later time, which permits the AGP graphics device 7a to pipeline C2 several access requests while waiting for data transfers to occur. As a result of pipelining, several read and/or write access requests may be simultaneously outstanding in request queues 100. Access requests can either be pipelined across an address/data bus (AD bus) 105, 107 of AGP 9 or transferred through sideband address lines 107 of AGP 9 and received by request queue 100.

Please replace the paragraph beginning at page 6, line 1 with the following amended paragraph:

Scheduler 102 processes the access requests in request queue 100. Read data are obtained from system memory 4 and are returned at the initiative of scheduler 102 through read data return queue 104 and across AD bus 105 of the AGP 9. Write data are provided by AGP C3 compliant graphics controller 7a at the direction of scheduler 102 when space is available in the write data queue 108. Thus, AGP transactions generally include interleaved access requests and data transfers.